I claim:

1. An asynchronous transfer mode switch comprising:

a set of *m* input ports to receive cells;

a set of *n* buffer groups, each buffer group comprising a set of buffers, where $n > m$;

an input-to-buffer switching module to switch a cell received at one of the *m* input ports to one of the *n* buffer groups;

a set of output ports;

and

an output switching module to switch cells stored in the sets of buffers within the buffer groups to the set of output ports.

2. The asynchronous transfer mode switch as set forth in claim 1, wherein the input-to-buffer switching module is a single stage *m* by *n* crossbar switch.

3. The asynchronous transfer mode switch as set forth in claim 1, wherein the input-to-buffer switching module is a multi-plane crossbar switch.

4. The asynchronous transfer mode switch as set forth in claim 1, wherein the output switching module is a single stage crossbar switch.

5. The asynchronous transfer mode switch as set forth in claim 1, wherein the output switching module is a multi-plane crossbar switch.

6. The asynchronous transfer mode switch as set forth in claim 1, wherein each buffer within the sets of buffers is a 1-cell buffer.

7. The asynchronous transfer mode switch as set forth in claim 1, wherein each buffer group comprises a set of *k* buffers, the input-to-buffer switching module further comprising:

a set of *n* 1 by *k* demultiplexers; and

at least one crossbar switch to switch a cell received at one of the *m* input ports to one of the set of *n* 1 by *k* demultiplexers;

wherein each 1 by *k* demultiplexer is coupled to one of the set of *n* buffer groups to store each cell switched by the at least one crossbar switch into one buffer.

8. The asynchronous transfer mode switch as set forth in claim 7, wherein each buffer within the sets of buffers is a 1-cell buffer.

9. The asynchronous transfer mode switch as set forth in claim 1, further comprising:

a first memory device to store *n* data structures, wherein there is a one-to-one correspondence between the data structures and the buffer groups, wherein each data

structure indicates buffers within its corresponding buffer group available for storing new cells.

10. The asynchronous transfer mode switch as set forth in claim 9, wherein the *n* data structures are bit-maps.

11. The asynchronous transfer mode switch as set forth in claim 9, further comprising:

a second memory device to store *nk* CNT field values, wherein there is a one-to-one correspondence between the CNT field values and the buffers, wherein a CNT field value indicates a number of output ports to read its corresponding buffer

12. The asynchronous transfer mode switch as set forth in claim 1, further comprising:

a first memory device to store buffer group addresses indicative of which buffer groups have a buffer available to store a new data cell.

13. The asynchronous transfer mode switch as set forth in claim 12, wherein the first memory device is a FIFO such that all stored buffer group addresses in the first memory device are indicative of buffer groups having at least one buffer available to store a new data cell.

14. The asynchronous transfer mode switch as set forth in claim 12, further comprising:

a second memory device to store *n* bit maps, wherein there is a one-to-one correspondence between the bit maps and the buffer groups, wherein each bit map indicates buffers within its corresponding buffer group available for storing new cells.

15. The asynchronous transfer mode switch as set forth in claim 14, further comprising:

a third memory device to store *nk* CNT field values, wherein there is a one-to-one correspondence between the CNT field values and the buffers, wherein a CNT field value indicates a number of output ports to read its corresponding buffer.

16. The asynchronous transfer mode switch as set forth in claim 15, wherein each buffer group comprises a set of *k* buffers, the input-to-buffer switching module further comprising:

a set of *n* 1 by *k* demultiplexers; and

at least one crossbar switch to switch a cell received at one of the *m* input ports to one of the set of *n* 1 by *k* demultiplexers;

wherein each 1 by *k* demultiplexer is coupled to one of the set of *n* buffer groups to store each cell switched by the at least one crossbar switch into one buffer.

17. A switching engine comprising:

a set of input ports to receive cells;

a set of buffer groups, each buffer group comprising a set of buffers, the set of buffer groups greater in number than the set of input ports;

an input-to-buffer switching module to switch cells received at the input ports to the sets of buffers within the set of buffer groups, wherein each switched cell is stored in one buffer within one buffer group;

a set of output ports; and

an output switching module to switch cells stored in the sets of buffers within the buffer groups to the set of output ports.

18. The switching engine as set forth in claim 17, further comprising:

a memory device to store buffer group addresses indicative of which buffer groups have a buffer available to store a new data cell, wherein all stored buffer group addresses in the memory device are indicative of buffer groups having at least one buffer available to store a new data cell.

19. The switching engine as set forth in claim 17, further comprising:

a memory device to store bit maps indicative of buffer states within the set of buffer groups.

20. The switching engine as set forth in claim 17, further comprising:

a memory device to store CNT field values corresponding to cells stored in the buffers within the set of buffer groups, wherein a CNT field value associated with a stored cell is indicative of a number of output ports to read the stored cell.

21. The switching engine as set forth in claim 17, further comprising:

a first memory device to store buffer group addresses indicative of which buffer groups have a buffer available to store a new data cell, wherein all stored buffer group addresses in the first memory device are indicative of buffer groups having at least one buffer available to store a new data cell;

a second memory device to store bit maps indicative of buffer states within the set of buffer groups; and

a third memory device to store CNT field values corresponding to cells stored in the buffers within the set of buffer groups, wherein a CNT field value associated with a stored cell is indicative of a number of output ports to read the stored cell.

22. The switching engine as set forth in claim 21, wherein the first memory device is a FIFO memory device.

23. A switching engine to switch cells from input ports to output ports, the switching engine comprising:

an input processing module to attach routing tags to cells;

a set of buffer groups, wherein each buffer group comprises a set of buffers to store cells; and

a buffer management module comprising a first memory device to store pointers to those buffer groups having at least one available buffer to store a new cell;

wherein the input processing module is coupled to the buffer management module to send buffer allocation requests to the buffer management module, wherein in response to a buffer allocation request the buffer management module shifts out a pointer stored in the first memory device.

24. The switching engine as set forth in claim 23, wherein the number of buffer groups within the set of buffer groups is greater than the number of input ports.

25. The switching engine as set forth in claim 23, wherein pointers shifted out of the first memory device are returned to the first memory device if and only if buffer groups pointed to by the shifted-out pointers have at least one available buffer to store a new cell.

26. The switching engine as set forth in claim 23, wherein each buffer group has a state indicative of which of its buffers are available to store a new cell, the buffer management module further comprising:

a second memory device to store bit maps indicative of the states of the set of buffer groups.

27. The switching engine as set forth in claim 26, the buffer management module further comprising:

a buffer allocation module to allocate buffers in response to buffer allocation requests, wherein the buffer allocation module receives a bit map stored in the second

memory device at a location indicated by the shifted-out pointer, provides a buffer number pointing to a bit position within the bit map indicative of an available buffer in the buffer group pointed to by the shifted-out pointer to store a new data cell, and updates the bit map by changing the bit position value to indicate a new state of the buffer group pointed to by the shifted-out pointer.

28. The switching engine as set forth in claim 27, wherein in response to the buffer allocation request, the buffer management module sends to the input processing module the shifted-out pointer and the buffer number, and the input processing module attaches a routing tag to a cell indicative of the shifted-out pointer and the buffer number.

29. The switching engine as set forth in claim 27, the buffer management module further comprising:

a return flag module to set a return flag associated with the shifted-out pointer to a first value if the new state indicates at least one available buffer in the buffer group pointed to by the shifted-out pointer, and to a second value different from the first value if the new state indicates no available buffers in the buffer group pointed to by the shifted-out pointer.

30. The switching engine as set forth in claim 29, wherein the first memory device is coupled to the return flag module to store the shifted-out pointer if and only if its associated return flag is the first value.

31. An asynchronous transfer mode switch comprising a switching engine to switch cells from input ports to output ports, the switching engine comprising:

an input processing module to attach routing tags to cells;

a set of buffer groups, wherein each buffer group comprises a set of buffers to store cells; and

a buffer management module comprising a first memory device to store pointers to those buffer groups having at least one available buffer to store a new cell;

wherein the input processing module is coupled to the buffer management module to send buffer allocation requests to the buffer management module, wherein in response to a buffer allocation request the buffer management module shifts out a pointer stored in the first memory device, wherein pointers shifted out of the first memory device are returned to the first memory device if and only if buffer groups pointed to by the shifted-out pointers have at least one available buffer to store a new cell.

32. The switching engine as set forth in claim 31, wherein the number of buffer groups within the set of buffer groups is greater than the number of input ports.